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(54) A semiconductor light emitting device.

(57) A semiconductor light emitting device (10) which allows part of an active layer (13) to generate light by supplying current to the part of the active layer (13) is disclosed. The semiconductor light emitting device (10) includes : a semiconductor substrate (11) having upper and lower surface, the upper surface having a stepped portion (11a), the stepped portion (11a) dividing the upper surface into a least a first area and a second area ; a current confining layer (20), formed on the upper surface of the substrate (11), the current confining layer (20) being discontinuous at the stepped portion (11a), the current flowing through an area between the first area and the second area of the substrate (11) ; a multilayer structure (12, 13, 14, 15) formed on the current confining layer (20), the multilayer structure (12, 13, 14, 15) including the active layer (13) ; a first electrode (17) which covers only part of an upper surface of the multilayer structure (12, 13, 14, 15) ; and a second electrode (18) formed over the lower surface of the substrate (11). In the semiconductor light emitting device, the light generated from the part of the active layer (13) is extracted to the outside through a portion of the upper surface of the multilayer structure (12, 13, 14, 15) which is not covered with the first lectrode (17).

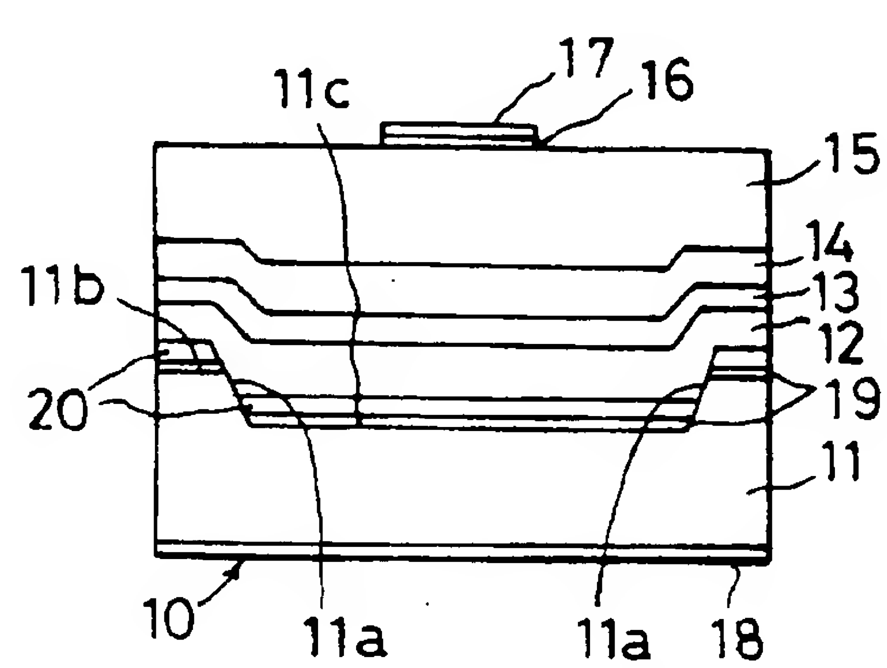

FIG.1A.

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BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a semiconductor light emitting device, and more particularly to a semiconductor light emitting device with which generated light can be effectively extracted to the outside.

2. Description of the Related Art:

Since light emitting diodes (hereinafter referred to as LEDs) have high reliability, they are used as light sources in various types of display apparatus as a substitute for a tungsten lamp. Furthermore, the LEDs have attracted much attention as display devices which are used indoors and outdoors. As the intensity of light emitted from the LED becomes higher, it is expected that the LED will be an alternative medium to a neon lamp in the future. In a few years, the outdoor display market of LEDs will remarkably progress. The high-intensity LED was first realized as an LED for emitting red light having a double heterostructure (DH) of GaAlAs system a few years ago.

Recently, a DH-type LED for emitting light of a band from orange to green of InGaAlP system has been made so as to be of a high-intensity type. In order to increase the luminous efficiency of such LEDs, it is important to increase the generating efficiency of light within the LED and also it is important to increase the extracting efficiency of the generated light to the outside.

Figures 10A and 10B show an exemplary LED of the prior art. The LED is an InGaAlP-system LED 100 capable of emitting light of a green band. Figure 10A is a transverse cross-sectional view of the LED 100 in which current flow is indicated by broken lines. Figures 10B is a transverse cross-sectional view of the LED 100 in which light generation is indicated by solid lines (a - d).

In the LED 100, an n-GaAs buffer layer 109 (thickness: 0.1 micrometers (μm)), an n-$In_{0.5}(Ga_{0.3}Al_{0.7})_{0.5}P$ carrier confining layer (cladding layer) 102 (thickness: 1.5 μm), a non-doped $In_{0.5}(Ga_{0.55}Al_{0.45})_{0.5}P$ active layer 103 (thickness: 0.7 μm), a p-$In_{0.5}(Ga_{0.3}Al_{0.7})_{0.5}P$ window layer (cladding layer) 104 (thickness: 1.5 μm), a p-$Ga_{0.3}Al_{0.7}As$ current diffusing layer 105 (thickness: 5 μm), and a p-GaAs ohmic contact layer 106 are grown on an n-GaAs substrate 101, in this order, by metal organic chemical vapor deposition (MOCVD).

An upper electrode 107 is formed on the p-GaAs ohmic contact layer 106. A lower electrode 108 is formed on th lower surface of the n-GaAs substrate 101. Th upp r electrode 107 and the und rlying ohmic contact layer 106 are formed by etching a peripheral portion thereof while leaving a portion having a size for lead bonding (width: about 70 μm) unetched. A current inject d from th upper lectrode 107 is diffused in the curr nt diffusing lay r 105 as indicated by the broken lines in Figur 10A. The diffused current is injected over the entire non-doped $In_{0.5}(Ga_{0.55}Al_{0.45})_{0.5}P$ active layer 103, so as to generate light.

In the LED 100, the current is injected over the entire non-doped $In_{0.5}(Ga_{0.55}Al_{0.45})_{0.5}P$ active layer 103, but a larger part of the injected current concentrates in a portion 103a directly under the upper electrode 107. As a result, an amount of light generated from the portion 103a is larger as compared with the remaining portion. Regarding light beams (a - c) which travel upwardly from the portion 103a directly under the upper electrode 107, the light beams are reflected from the upper electrode 107, as is shown in Figure 10B. Accordingly, the light beams are not extracted to the outside. Regarding light beams which travel upwardly but obliquely, if a light beam (d) is incident on an upper face 105a at a critical angle or a larger angle, the light beam is not extracted to the outside, either. Therefore, the larger part of the current injected to the active layer 103 is disadvantageously consumed for generating light which cannot be extracted.

SUMMARY OF THE INVENTION

The semiconductor light emitting device of this invention which allows part of an active layer to generate light by supplying current to a part of the active layer, includes: a semiconductor substrate having upper and lower surface, the upper surface having a stepped portion, the stepped portion dividing the upper surface into at least a first area and a second area; a current confining layer, formed on the upper surface of the substrate, the current confining layer being discontinuous at the stepped portion, the current flowing through an area between the first area and the second area of the substrate; a multilayer structure formed on the current confining layer, the multilayer structure including the active layer; a first electrode which covers only part of an upper surface of the multilayer structure; and a second electrode formed over the lower surface of the substrate, wherein the light generated from the part of the active layer is extracted to the outside through a portion of the upper surface of the multilayer structure which is not covered with the first electrode.

Thus, the invention described herein makes possible the advantage of providing a semiconductor light emitting device with excellent intensity in which a light emitting portion of an active layer is defined as a portion excluding a portion directly under an upper electrode, and a construction of which is designed to easily extract the generated light from the upper side, whereby the light extraction efficiency is increased.

This and other advantag s of the present inven-

tion will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B are schematic views showing an exemplary construction of a semiconductor light emitting device according to the invention. Figure 1A is a cross-sectional view of an LED and Figure 1B is a view showing current flow and light generation.

Figures 2A to 2D are schematic views showing a manufacturing process of the semiconductor light emitting device of the invention.

Figures 3A and 3B are plan views each showing a surface shape of the LED of Figure 1A.

Figures 4A and 4B are schematic views showing another construction of a semiconductor light emitting device according to the invention. Figure 4A is a cross-sectional view of an LED in Figure 4B is a view illustrating current flow and light generation.

Figure 5 is a cross-sectional view showing another construction of a semiconductor light emitting device according to the invention.

Figures 6A and 6B are schematic views showing another construction of a semiconductor light emitting device according to the invention. Figure 6A is a cross-sectional view of an LED and Figures 6B is a view illustrating current flow and light generation.

Figure 7 is a cross-sectional view showing another construction of a semiconductor light emitting device according to the invention.

Figure 8 is a cross-sectional view showing still another construction of a semiconductor light emitting device according to the invention.

Figure 9 is a plan view showing an upper electrode shown in Figure 8.

Figures 10A and 10B are schematic views showing an exemplary construction of a conventional LED. Figure 10A is a cross-sectional view illustrating current flow in the LED, and Figure 10B is a cross-sectional view illustrating light generation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a semiconductor light emitting device of the invention will be described by way of examples and with reference to the drawings. Figures 1A and 1B show a semiconductor light emitting device (LED) 10. Figure 1A is a transverse cross-sectional view of the LED 10. Figure 1B is a cross-sectional view illustrating current flow and light generation.

The LED 10 includes a multilayer structure on an n-GaAs substrate 11. In the multilayer structure, an n-GaAs buffer layer 19, a p-GaAs current confining layer 20, an n-InGaAlP carrier confining layer (cladding lay r) 12, an InGaAlP activ layer 13, a p-InGaAlP window layer (cladding layer) 14, a p-GaAlAs current diffusing layer 15, and a p-GaAs contact layer 16 are formed, in this order.

An upper electrode 17 is deposited on an upper surface of the p-GaAS contact layer 16. A lower electrode 18 is deposited on a lower surface of the n-GaAs substrate 11. The upper electrode 17 and the p-GaAs contact layer 16 are formed on a center portion of an upper surface of the p-GaAlAs current diffusing layer 15.

An upper surface of the n-GaAs substrate 11 has a recess. This means that the upper surface of the n-GaAs substrate 11 is constituted by a high-level plane (a higher portion 11b), a low-level plane (a lower portion 11c) and a slope for joining the portions of different levels (a stepped portion 11a). The higher portion 11b corresponds to a peripheral portion of the upper surface of the n-GaAs substrate 11. Only on the higher portion 11b and the lower portion 11c, an n-GaAs buffer layer 19 and a p-GaAs current confining layer 20 are grown. In other words, the n-GaAs buffer layer 19 and the p-GaAs current confining layer 20 are formed so as to have discontinuity at the stepped portion 11a.

On the p-GaAs current confining layer 20, the n-InGaAlP carrier confining layer (cladding layer) 12, the InGaAlP active layer 13, the p-InGaAlP window layer (cladding layer) 14, and the p-GaAlAs current diffusing layer 15 are sequentially formed.

The plan shape of the lower portion 11c is square, the same as the plan shape of the upper electrode 17. However, the lower portion 11c is sufficiently larger than the upper electrode 17. As a result, a portion 20a of the current confining layer 20 of a second conductivity type directly under the upper electrode 17 is located within the range of the lower portion 11c. Moreover, the current confining layer 20 on the lower portion 11c is formed without discontinuity.

Now, a fabrication process of the above semiconductor light emitting device is described with reference to Figures 2A to 2D.

First, as is shown in Figure 2A, a stepped portion having a level difference of 2 μm is formed in the n-GaAs substrate 11. In this example, a (100) plane substrate is used as the n-GaAs substrate 11. The stepped portion is formed, for example, in the following manner. First, a photoresist layer is formed to cover the upper surface of the n-GaAs substrate 11. Then, only an exposed area of the upper surface of the n-GaAs substrate 11 is etched, so as to form a recess in the n-GaAs substrate 11.

Next, as is shown in Figure 2B, the n-GaAs buffer layer 19 and the p-GaAs current confining layer 20 are sequentially formed on the n-GaAs substrate 11. In this formation, the crystal growth conditions for the layers 19 and 20 are adjusted such that the n-GaAs buffer layer 19 and the p-GaAs current confining lay-

er 20 are discontinuous at the stepped portion 11a. That is, the lay rs 19 and 20 are selectively grown on the higher portion 11b and the lower portion 11c. In this example, the crystal growth is carried out at a temperature of 720°C and at a pressure of 76 Torr. The n-GaAs buffer layer 19 and the p-GaAs current confining layer 20 are formed by MOCVD. In this example, the thicknesses of the n-GaAs buffer layer 19 and the p-GaAs current confining layer 20 are set to be 0.1 μm and 1 μm, respectively, both on the higher portion 11b and on the lower portion 11c of the n-GaAs substrate 11, by adjusting the crystal growth conditions for the layers 19 and 20. In this fabrication process, the current confining structure is easily formed in a self-alignment manner with the stepped structure of the n-GaAs substrate 11.

Then, the n-InGaAlP carrier confining layer (cladding layer) 12 is formed so as to have different thicknesses on the higher portion 11b and on the lower portion 11c. The thickness of the layer 12 on the lower portion 11c is larger than that on the higher portion 11b in order not to have discontinuity at the stepped portion 11a. In this example case, as is shown in Figure 2C, the thickness of the layer 12 on the higher portion 11b is 1.5 μm, and the thickness of the layer 12 on the lower portion 11c is 3.0 μm.

The InGaAlP active layer 13 is formed in such a manner that the thickness thereof on the lower portion 11c is 1 μm and the thickness thereof on the higher portion 11b is 0.8 μm. The p-InGaAlP window layer (cladding layer) 14 is formed in such a manner that the thickness thereof on the lower portion 11c is 1.5 μm, and the thickness thereof on the higher portion 11b is 1.3 μm. The p-GaAlAs current diffusing layer 15 is formed, as is shown in Figure 2D, in such a manner that the thickness thereof on the lower portion 11c is 5 μm, and the thickness thereof on the higher portion 11b is 4.9 μm. The p-GaAs contact layer 16 is formed to have a thickness of 0.2 μm. The upper electrode 17 and the p-GaAs contact layer 16 are etched to leave a center portion having a width of about 70 μm for lead bonding unetched.

According to the LED 10 of this example, a current from the n-GaAs substrate 11 is injected into the multilayer structure through the stepped portion 11a where the p-GaAs current confining layer 20 is discontinuous, as is indicated by the broken lines in Figure 1B. Since the upper electrode 17 is formed at the center of the multilayer structure, a larger part of the current is injected into a portion 13b of the active layer 13. The portion 13b is a remaining portion of the active layer 13 formed on the lower portion 11c excluding a portion 13a directly under the upper electrode 17. Light is efficiently generated in the remaining portion 13b of th activ layer 13, as is indicated by the solid lines in Figure 1B. Therefore, the generated light can be extracted upwardly from the upper fac of the multilayer structur without being stopped by th upper el ctrode 17. Thus, a light emitting diod having good light extraction efficiency can b provided.

The plan shapes of the upper electrode 17, the stepped portion 11a and the light generating portion 13b of the active layer 13 may be rectangular as is shown in Figure 3A, and alternatively may be circular as is shown in Figure 3B.

When the LED 10 shown in Figures 1A and 1B was mounted on a lamp having a diameter of 5 mm by molding, a light intensity of 3 candela (cd) can be obtained at a wavelength of 555 nm at 20 mA.

Figures 4A and 4B show another example of a semiconductor light emitting device according to the invention.

In an LED 30 of this example, a p-GaAs substrate 31 is used instead of the n-GaAs substrate 11 of the first example. Accordingly, all the layers in this example are of conductivity types opposite to those in the first example.

The shape of a stepped portion 31a of the p-GaAs substrate 31 is defined by higher portions 31b positioned in a peripheral portion and directly under an upper electrode 37 of the p-GaAs substrate 31, and by a lower portion 31c positioned between the higher portions 31b. There are two slopes for joining the higher portions 31b and the lower portion 31c, and the two slopes are opposite to each other.

Also, in the LED 30 of this example, an n-GaAs current confining layer 40 is formed so as to have discontinuity at an inner stepped portion 31a. A current is also injected through this discontinuous portion, as is indicated by the broken lines in Figure 4B. A larger part of the current is efficiently injected into a portion excluding the central higher portion 31b directly under the upper electrode 37. Therefore, in this example, the light extraction efficiency is good, as in the first example.

In the LED 30 of this example, a light intensity of 3.2 cd can be obtained at a wavelength of 567 nm (5 mmø, 20 mA). Alternatively, as is shown in Figure 5, an additional upper electrode 37 may be formed on a peripheral portion of an upper surface of the multilayer structure.

Figures 6A and 6B show still another example of a semiconductor light emitting device according to the invention. Figure 6A is a transverse cross-sectional view. Figure 6B is a cross-sectional view illustrating current flow and light generation.

An LED 30 of this example has substantially the same construction as that of the LED 30 shown in Figures 4A and 4B, except that the LED 30 of this example has no n-GaAlAs current diffusing layer. In the LED 30 of this example, an n-InGaAlP window layer (cladding layer) 34 having stepped portions 34a is formed as an upp rmost lay r. As is shown in Figure 6B, light generated from an active layer 33 can efficiently b extracted through the stepped portions 34a.

Figure 7 shows still anoth r example of a s miconductor light emitting d vic according to th present invention. An LED 30 of this example has substantially the same construction as that of the LED 30 shown in Figures 4A and 4B, except for the following differences. The differences are in that the LED 30 shown in Figure 7 has a layer 41' which is referred to as a light reflecting layer on a current confining layer 40, and in that the LED 30 shown in Figure 7 is not provided with a current diffusing layer. An exemplary case where the construction of Figure 7 is formed of AlGaAs system materials will be described.

In the LED 30 of Figure 7, on a p-GaAs substrate 31, a p-GaAs buffer layer 39, an n-GaAs current confining layer 40, the light reflecting layer 41' of p-type or n-type $Ga_{0.5}Al_{0.5}As/AlAs$ (ten layers), a p-$Ga_{0.3}Al_{0.7}As$ carrier confining layer (cladding layer) 32', a non-doped $Ga_{0.62}Al_{0.38}As$ active layer 33', an n-$Ga_{0.3}Al_{0.7}As$ window layer (cladding layer) 34', and an n-GaAs ohmic contact layer 36 are layered, in this order. An upper electrode 37 is deposited on an upper surface of the n-GaAs ohmic contact layer 36. A lower electrode 38 is deposited on the lower surface of the p-GaAs substrate 31.

In the LED 30 of this example, a current is injected in the same way as in the second example. However, generated light beams which travel downwardly are reflected upwardly by the light reflecting layer 41' and can be extracted to the outside, as is shown in Figure 7. As to the LED 30 of this example, when it is mounted on a lamp having a diameter of 5 mm, a light intensity of 10 cd can be obtained at a wavelength of 655 nm (red) at 20 mA. If twenty layers of $In_{0.5}(Ga_{0.5}Al_{0.5})_{0.5}P$ and InAlP are alternately layered, the light reflecting layer of this example can be applied to the LEDs of the InGaAlP system described in the first through fourth examples.

Figure 8 shows a sixth example of a semiconductor light emitting device according to the invention. In Figure 8, the injection of current is indicated by the broken lines, and the traveling of generated light is indicated by the solid lines. In a LED 30 of the sixth example, the structure of grown layers is substantially the same as those in the first and second examples except for the following differences. The differences are in that the structure of this example is provided with a light reflecting layer 41 as in the fifth example, and in that a number of stepped portions 31a are formed so as to provide multiple current injecting portions as light emitting portions. As is shown in Figure 9, the surface of the upper electrode 37 has a multi-stripe shape, and at the center of the surface of the upper electrode 37, a central electrode 37a is formed. In the LED 30 of this exampl , the current is uniformly injected into the multiple light mitting portions, and th h at which is generat d due to the current injection and the light generation is distributed. Accordingly, the luminous efficiency of the LED 30 is further increased and the reliability thereof is nhanced. In th LED 30 of this example, a light intensity of 5 cd can be obtained at a wavelength of 55 nm (5mm , 20 mA).

The material systems used in the examples of the invention are not limited to the InGaAlP system and the GaAlAs system which are described above. Alternatively, the material system may be a ZnSSe system, a CdZnS system, or the like. The conductivity type of the substrate is not specified, i.e., a p-type or n-type one is appropriately used. The conductivity types of the grown layers can be determined in accordance with the selected conductivity type of the substrate. The employed method of growth may alternatively be an LPE method, an MBE method, an ALE method, a CBE method, or the like, other than the MOCVD method. The current diffusing layer and the ohmic contact layer is not necessarily provided. These two layers may not be fabricated as far as the resistance is not high.

According to the invention, on a substrate of a first conductivity type having a stepped portion, a current confining layer of a second conductivity type is formed in such a manner that the layer is discontinuous at the stepped portion. On the current confining layer, a carrier confining layer (cladding layer) of the first conductivity type, an active layer, and a window layer (cladding layer) of the second conductivity type are formed. Directly under an upper electrode, the current confining layer of the second conductivity type is formed without discontinuity. Therefore, a current is injected into the remaining portion of the active layer excluding a portion of the active layer directly under the upper electrode, through the discontinuous portion of the current confining layer formed on the substrate. A light generating portion of the active layer corresponds to the portion excluding the portion directly under the upper electrode, whereby the generated light can easily be extracted. Therefore, the light extraction efficiency of the generated light is improved. Thus, a light emitting diode with excellent light intensity can be provided.

This invention provides a short-wavelength and high-intensity LED for emitting light of a band from orange to green, and which can be applied to an LED for emitting light of a band from infrared to red.

Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

Claims

1. A semiconductor light emitting device which allows part of an active layer to generat light by

supplying current to said part of said activ layer, said d vice comprising:

a semiconductor substrate having upper and lower surface, said upper surface having a stepped portion, said stepped portion dividing said upper surface into at least a first area and a second area;

a current confining layer, formed on said upper surface of said substrate, said current confining layer being discontinuous at said stepped portion, said current flowing through an area between said first area and said second area of said substrate;

a multilayer structure formed on said current confining layer, said multilayer structure including said active layer;

a first electrode which covers only part of an upper surface of said multilayer structure; and

a second electrode formed over said lower surface of said substrate,

wherein said light generated from said part of said active layer is extracted to the outside through a portion of said upper surface of said multilayer structure which is not covered with said first electrode.

2. A semiconductor light emitting device according to claim 1, said device further comprising a light reflecting layer formed on said current confining layer,

wherein said light reflecting layer reflects part of said light generated from said part of said active layer which is incident on said light reflecting layer to the outside.

3. A semiconductor light emitting device according to claim 1, wherein said semiconductor substrate has a recess formed in a portion of said upper surface thereof, said first area of said upper surface corresponding to a bottom face of said recess, said second area of said upper surface corresponding to a portion of said upper surface excluding said portion of said recess, and

wherein said first electrode is positioned above said first area, the size of said first electrode being smaller than that of said first area.

4. A semiconductor light emitting device according to claim 1, wherein said upper surface has a plurality of stepped portions, thereby providing a plurality of parts for generating light in said active layer, and

wherein said first electrode having a shape which does not cover said parts for generating light.

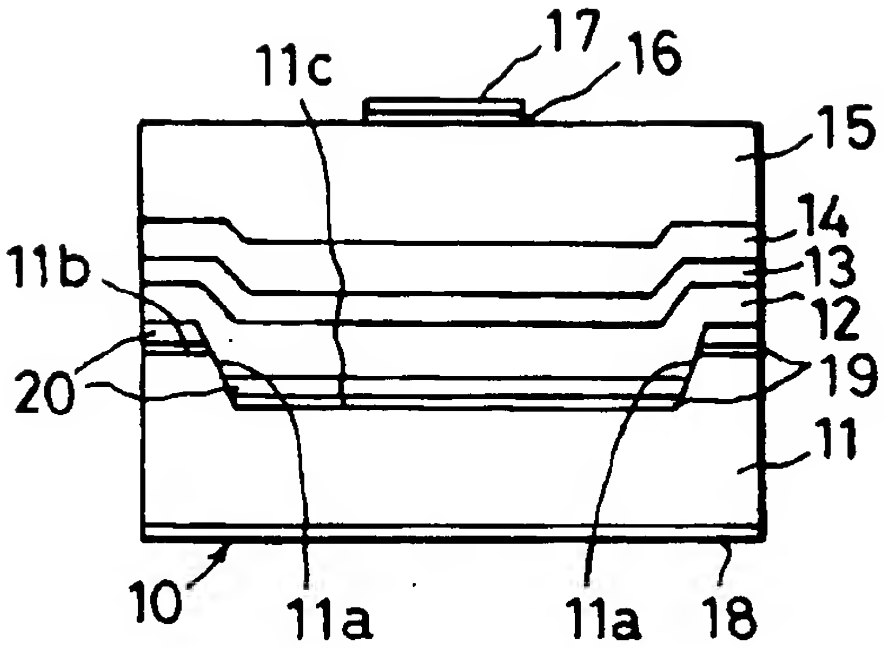

FIG.1A.

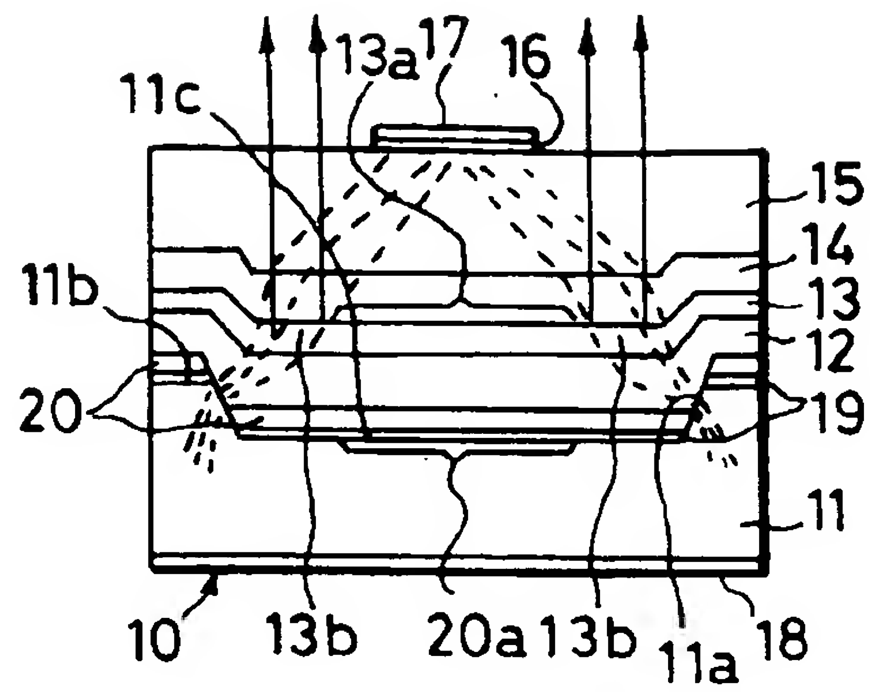

FIG.1B.

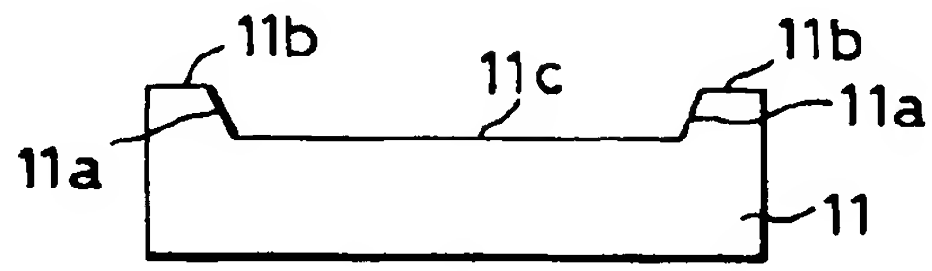

FIG.2A.

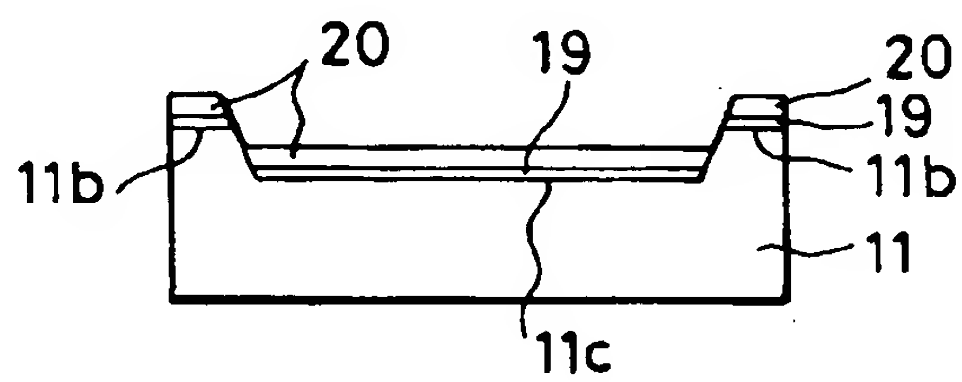

FIG.2B.

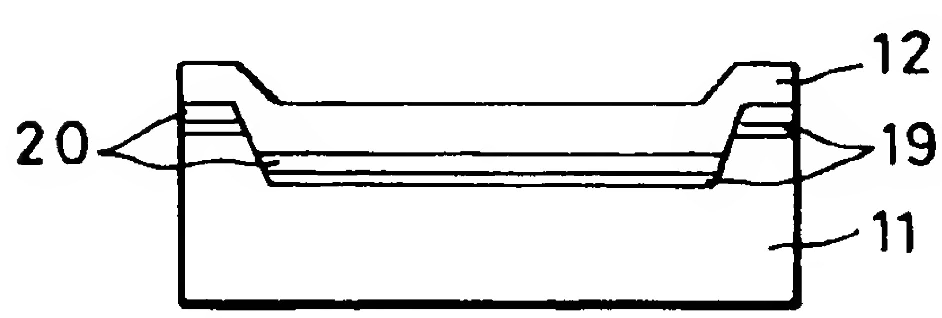

FIG.2C.

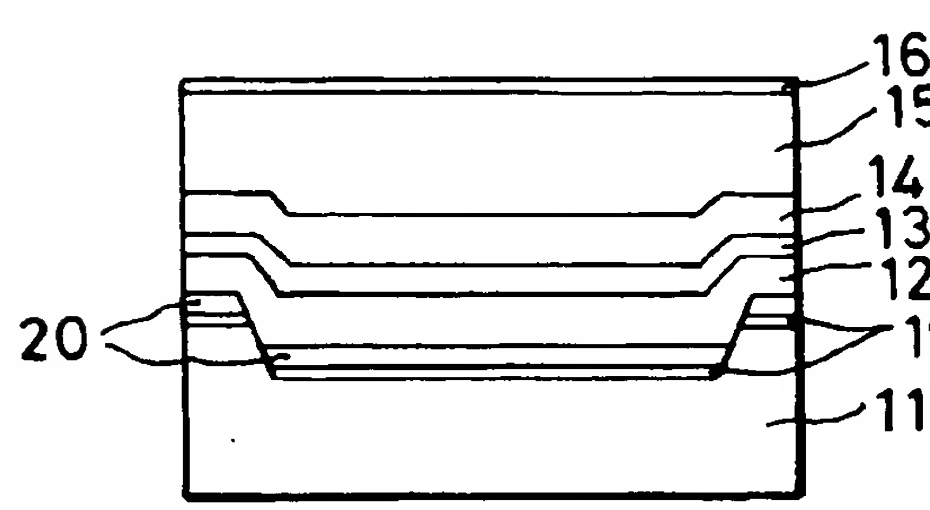

FIG.2D.

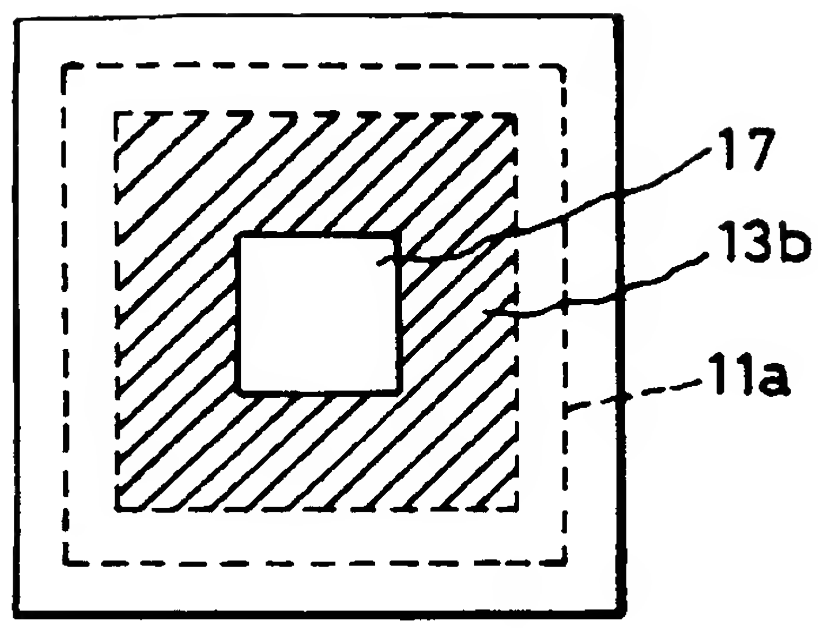

FIG.3A.

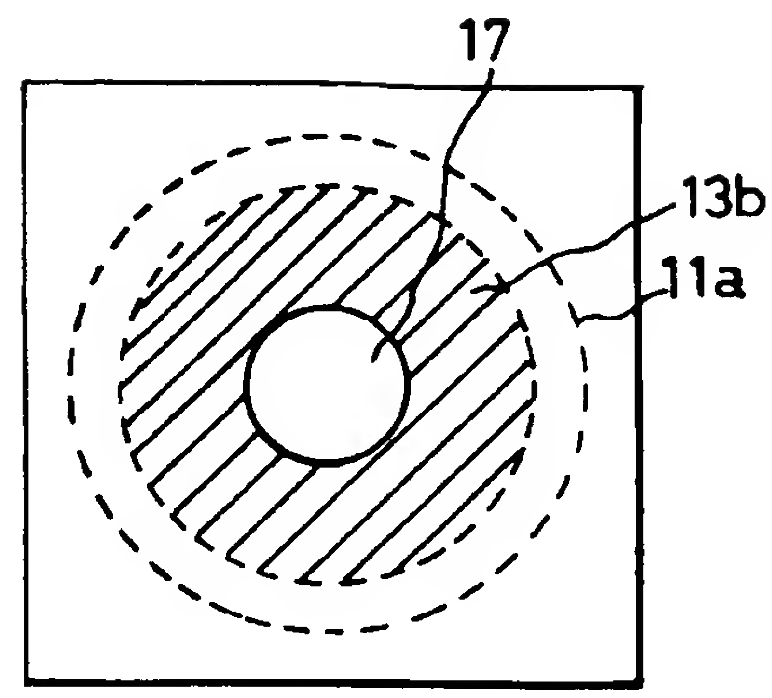

FIG.3B.

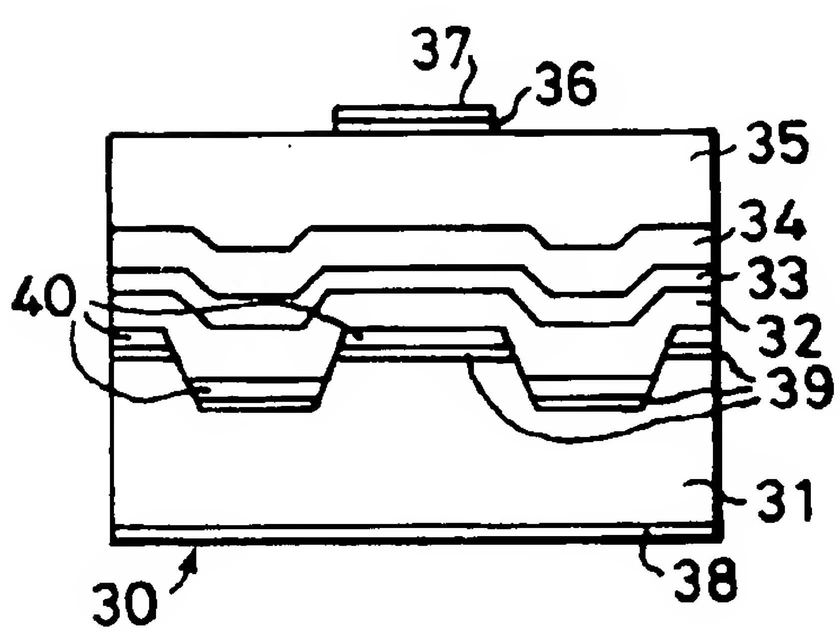

FIG.4A.

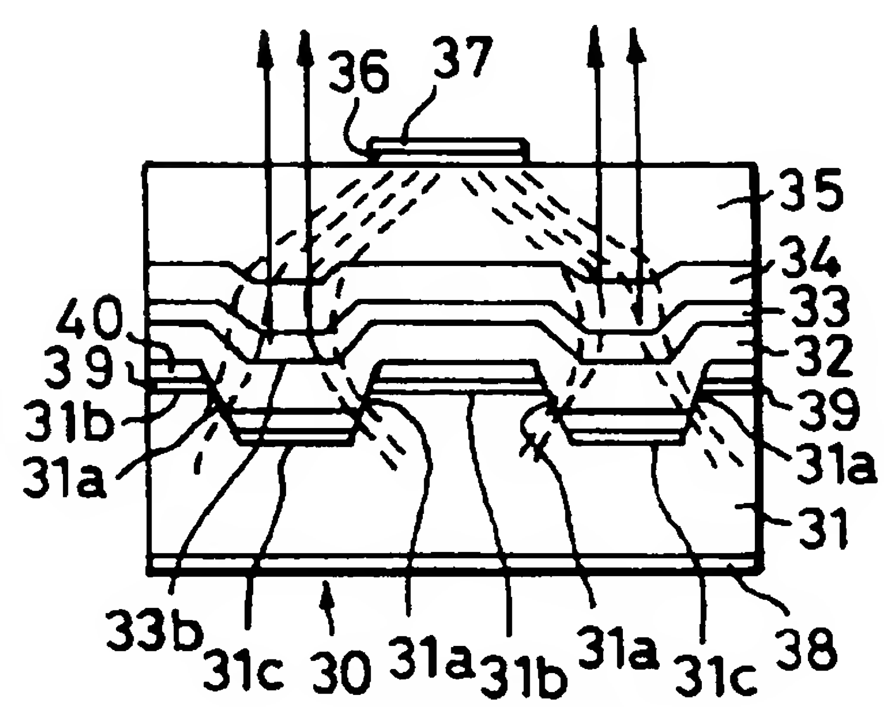

FIG.4B.

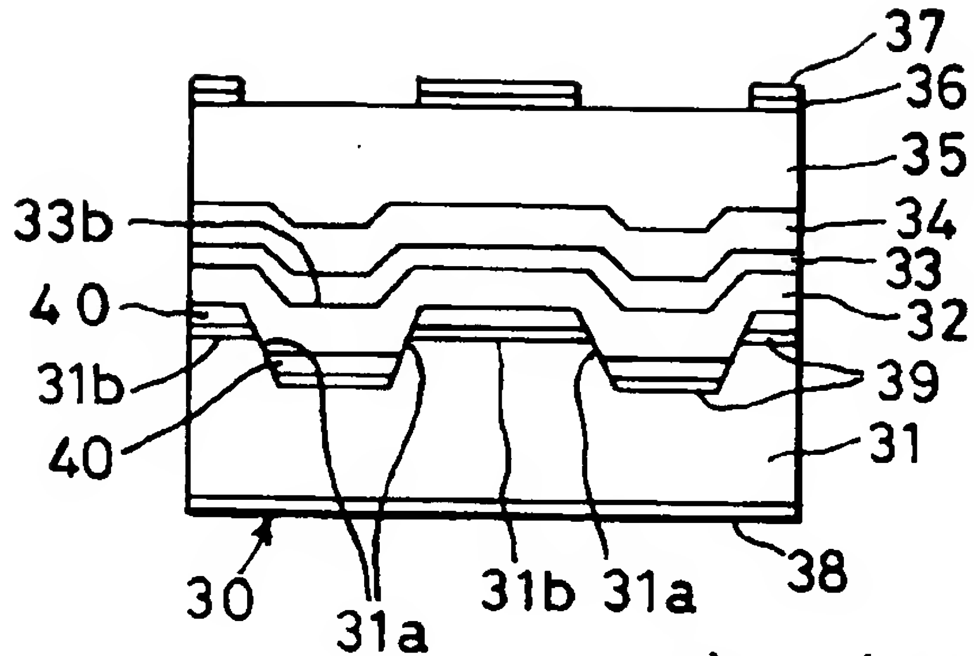

FIG.5.

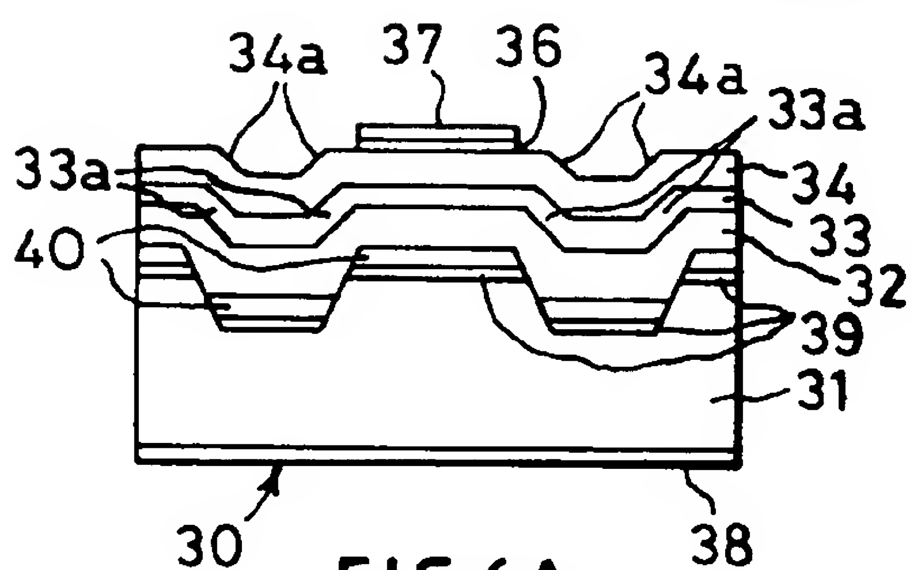

FIG.6A.

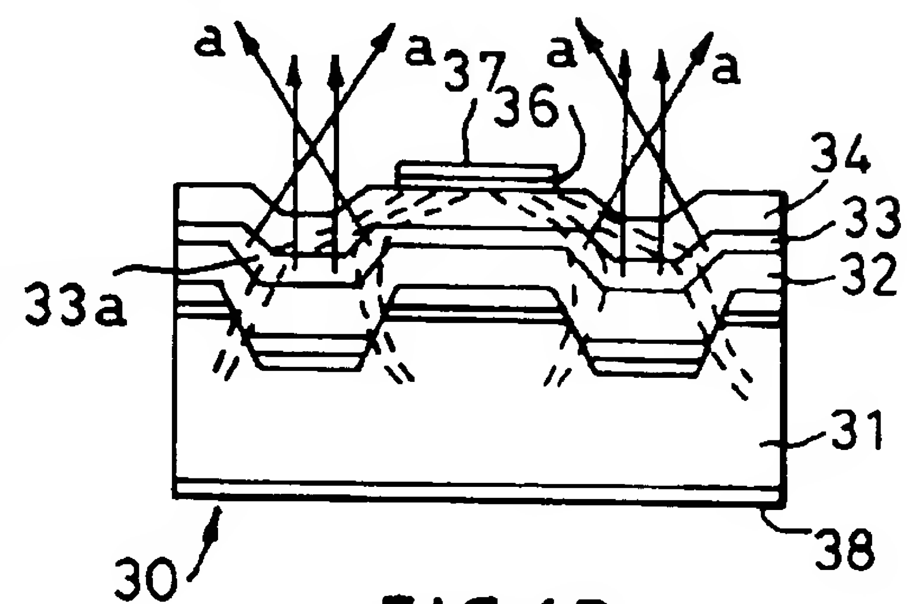

FIG.6B.

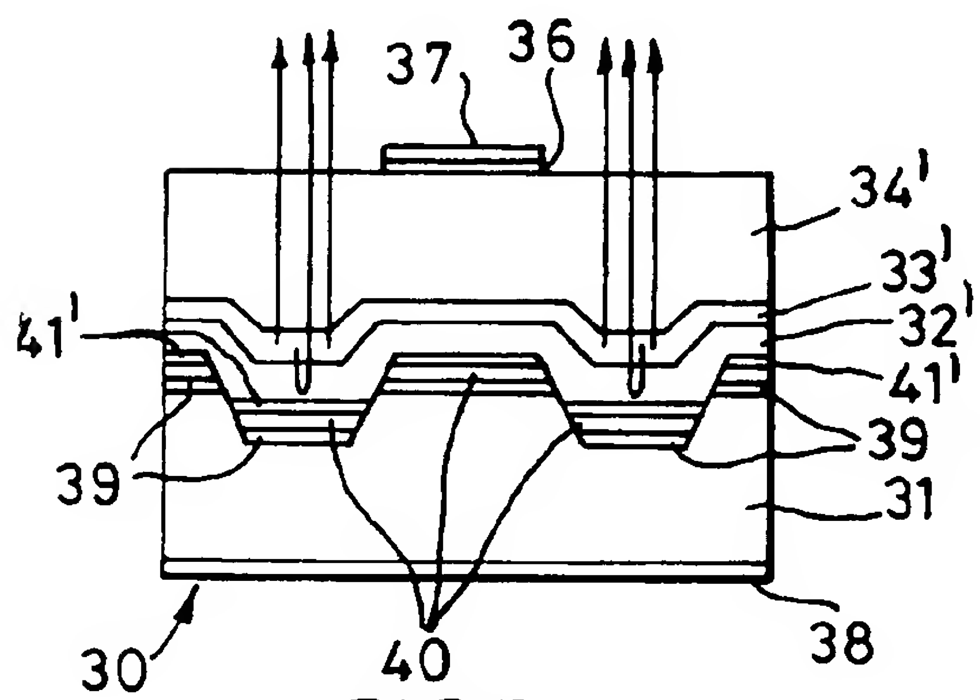

FIG.7.

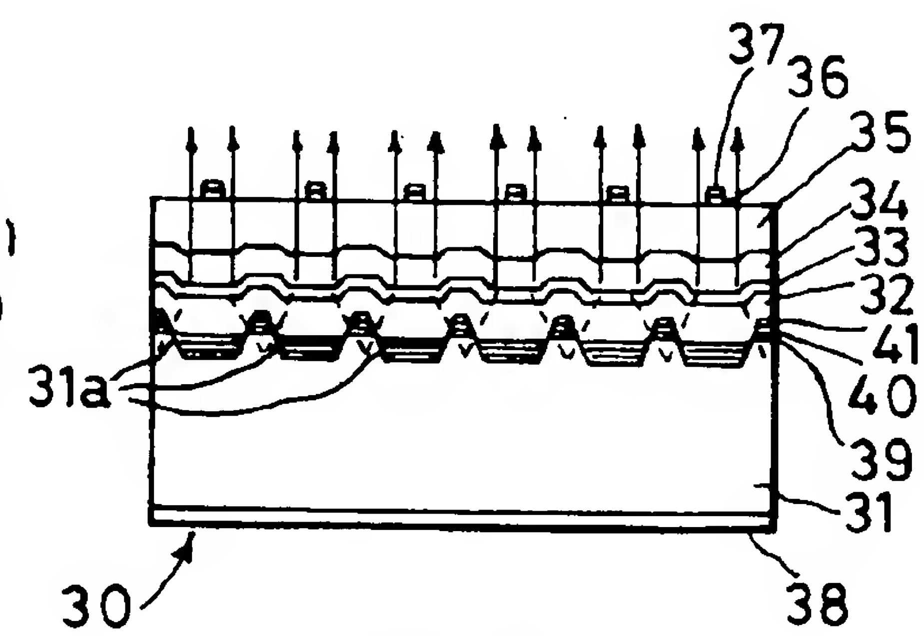

FIG.8.

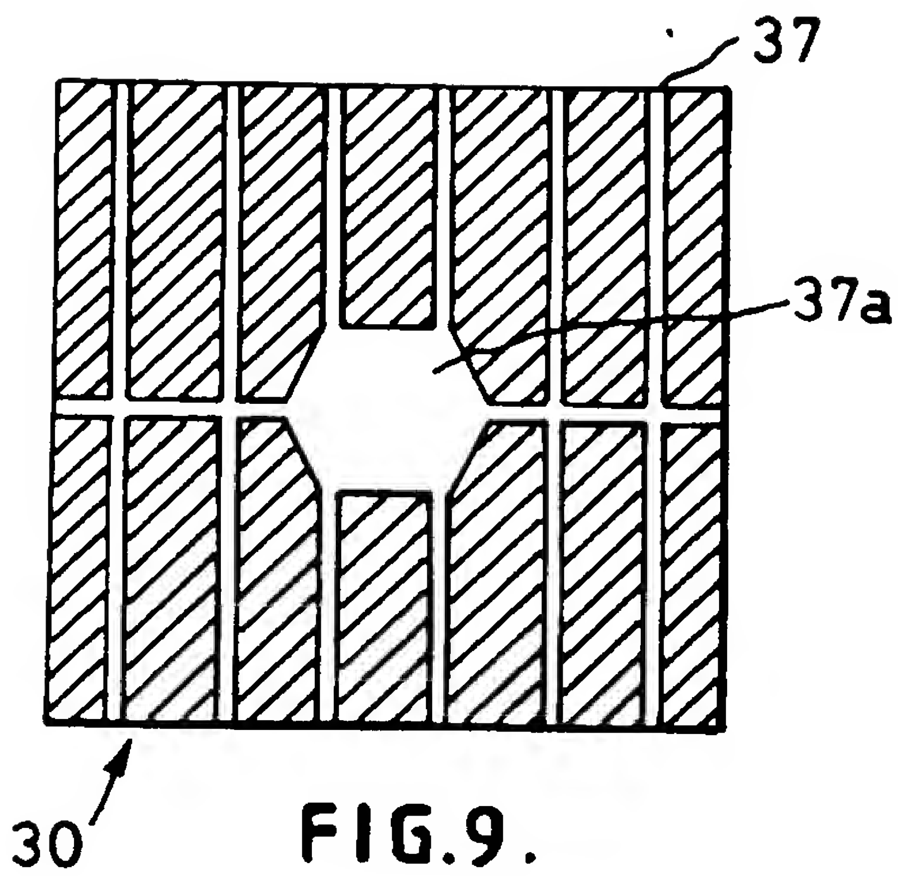

FIG.9.

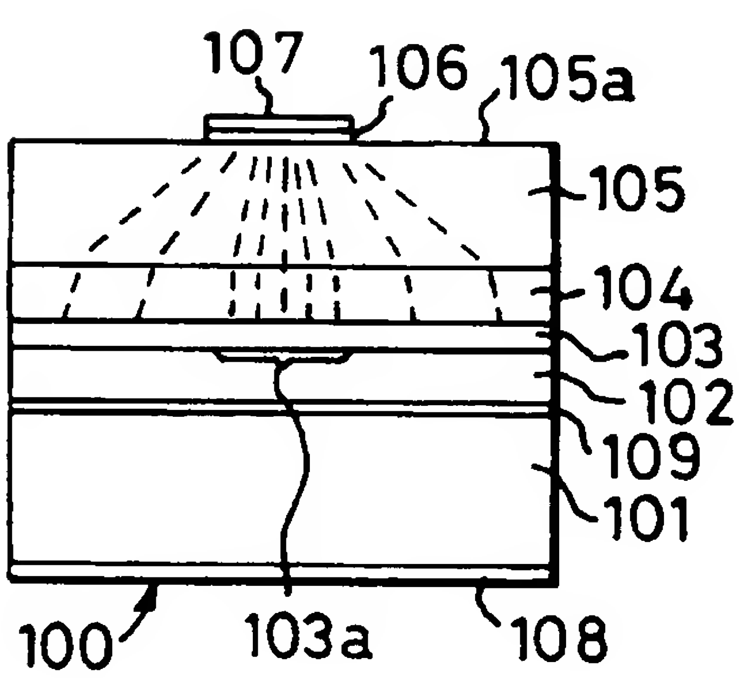

FIG.10A.

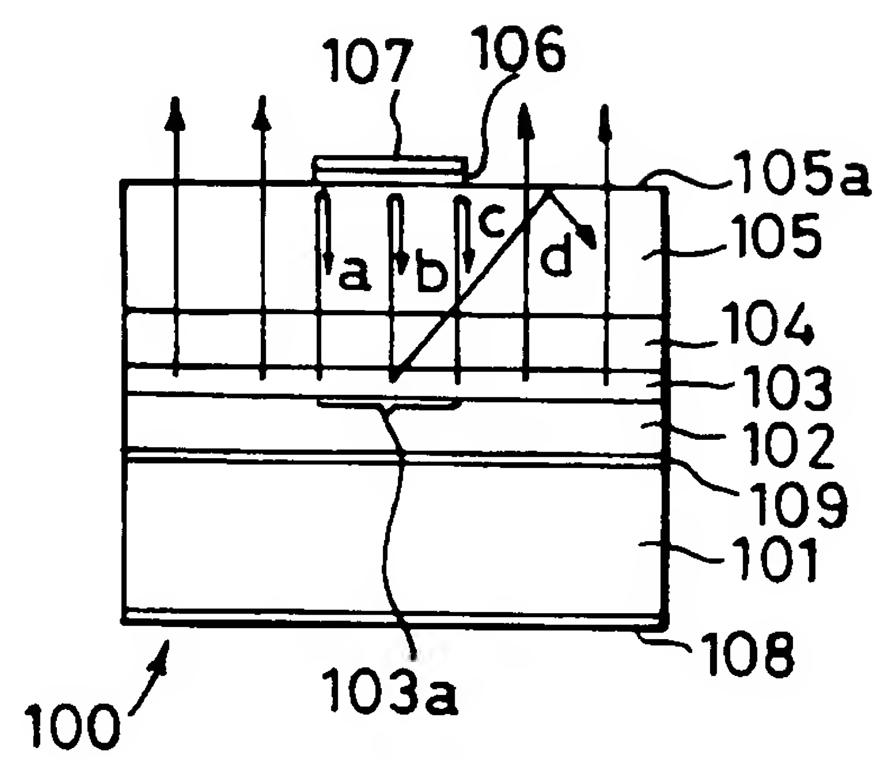

FIG.10B.

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EUROPEAN SEARCH REPORT

Application Number
EP 93 30 1623

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X A	GB-A-2 053 564 (SUMITOMO ELECTRIC INDUSTRIES LTD.) * page 2, line 33 - line 92 * * page 3, line 37 - line 45; figure 4 * ---	1 3	H01L33/00
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 91 (E-394)9 April 1986 & JP-A-60 235 486 (MATSUSHITA DENKI SANGYO KK) 22 November 1985 * abstract * ---	1,3	
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 89 (E-309)18 April 1985 & JP-A-59 219 976 (MITSUBISHI DENKI KK) 11 December 1984 * abstract * ---	1,3	
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 330 (E-655)7 September 1988 & JP-A-63 093 188 (MITSUBISHI ELECTRIC CORP) 23 April 1988 * abstract * ---	1,3	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	EP-A-0 430 041 (DAIDO TOKUSHUKO KABUSHIKI) * abstract; figures * ---	1,2	H01L
A	DE-A-4 017 632 (KABUSHIKI KAISHA TOSHIBA) * abstract; figures * -----	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	11 MAY 1993	DE LAERE A.L.

CATEGORY OF CITED DOCUMENTS

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